ViPro Status (09/24/12)

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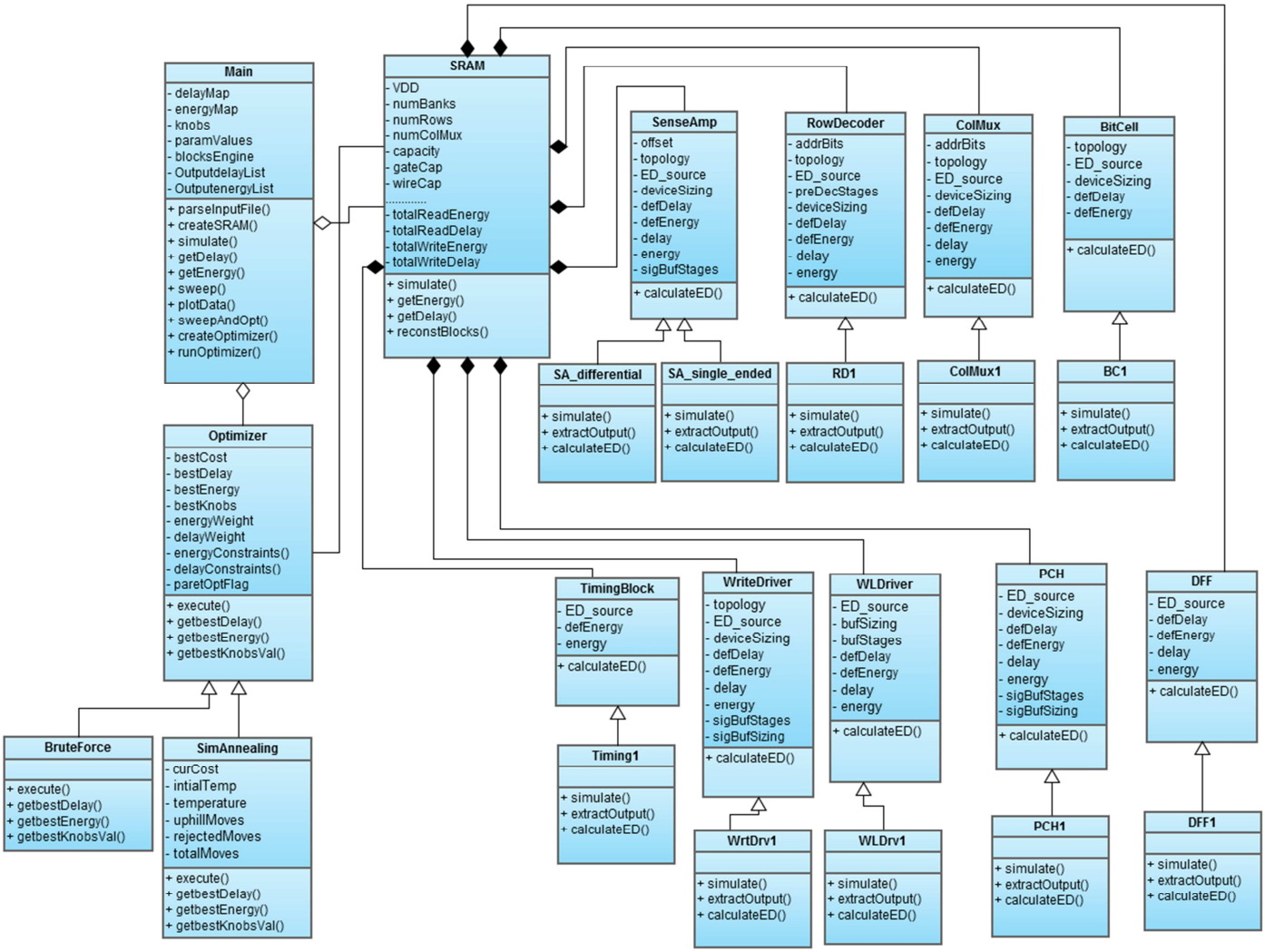
Contents

UML Diagram

The latest version of ViPro is written in C++, provide hierarchical implementation of the SRAM structure and scalability. The current supported optimization algorithm is random search simulated annealing as shown in the UML class diagram below.



Current Status

Design Exploration

[1] Calculate the E/D for a certain SRAM structure.

[2] Allow sweeping architecture-level parameters (number of rows, colMux, banks) and evaluate the total energy and delay at each point.

[3] Allow sweeping sense amp (SA) offset voltage for a fixed SRAM structure

[4] Allow sweeping pre-charge device sizing.

Design Optimization

[1] Optimize architectural level (number of rows, colMux, banks)

[2] Optimize design with and without using assist features (word-line boosting)

[3] Optimize decoder sizing

[4] Optimize sense amp, pre-charge devices, word-line driver sizing for a fixed SRAM structure.

Future Plan

[1] Sub-Block optimization to be handled using convex optimization (SCOT).

[2] Support optimization of non-CMOS SRAM arrays (STTRAM, FRAM).

[3] Support register-file optimization.

[4] Expanding metrics of optimization (yield, stability, area).